



**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

501.39932X00

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TECHNOLOGY CENTER 2200

2811  
#19 8-27-03  
IDS  
Examiner

Applicants: J. NOGUCHI, et al.

Application No.: 09/825,946

Filed: April 5, 2001

For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND  
FABRICATION METHOD FOR SEMICONDUCTOR  
INTEGRATED CIRCUIT DEVICE

Art Group: 2811

Examiner: H. Vu

**INFORMATION DISCLOSURE STATEMENT  
UNDER 37 C.F.R. §1.97 AND §1.98**

Assistant Commissioner of Patents  
Washington, D.C. 20231

April 29, 2003

Sir:

In the matter of the above-identified application, applicants submit herewith a copy of the documents listed in the attached form equivalent to Form PTO-1449 for the Examiner's consideration.

This Information Disclosure Statement is being submitted before the mailing date of a notice of allowance and is accompanied by the fee of \$180.00 set forth in 37 C.F.R. §1.17(p).

Each of the documents listed on the attached form equivalent to Form PTO-1449 is in the English language.

It is respectfully requested that this information disclosure statement be considered by the Examiner.

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Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (501.39932X00) and please credit any excess fees to such Deposit Account.

Respectfully submitted,

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